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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention is applied to a semiconductor device and relates to effective technology.
[0002]
[Description of the Prior Art] The conventional semiconductor device has what generally connected the semiconductor chip with the internal lead with the wire, and the thing to connect by the bump, and these the external leads of both have the structure which projected from the side of the closure resin section of a semiconductor device. Moreover, for example, there are some which are being exposed from the closure resin section by considering the field (rear face of an internal lead) where an internal lead is connected with a semiconductor chip by the bump, and the bump is not connected as an external lead like the semiconductor device indicated by JP,5-129473,A and JP,5-25158,A. [0003]
[Problem(s) to be Solved by the Invention] this invention person found out the following troubles, as a result of examining the above-mentioned conventional technology.
[0004] The need of reducing the size of the substrate in which a semiconductor device is carried etc. with downsizing of the system instrument which used the semiconductor device in recent years came out. For this reason, the mounting efficiency of a substrate was raised by reducing the size of a semiconductor device etc., and substrate size has been reduced.
[0005] Reduction of this semiconductor device was mainly made by reduction of a semiconductor chip, and the external lead was not set as the object of the reduction.
[0006] For this reason, the present condition is that the cure against reduction in the area which the external lead of the semiconductor device on a substrate occupies is not made.
[0007] Therefore, since the external lead in the conventional semiconductor device had the structure which generally projected from the side of the closure resin section of a semiconductor device, only the part of the external lead which projected from the side of the closure resin section took the component-side product too much, and it had the trouble that the mounting efficiency in substrate mounting was bad.
[0008] The purpose of this invention is to offer the technology which can be improved in the mounting efficiency in substrate mounting of a semiconductor device.
[0009] The other purposes and the new feature will become clear by description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0010]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0011] The semiconductor chip by which a resin seal is carried out, and two or more leads with which the external lead portion and the internal lead portion were united, The 1st field where it is a semiconductor device possessing the resin-seal section, and the above-mentioned lead counters with a semiconductor chip, Have the 2nd field used as the rear face of this 1st field, and the internal lead portion of the 1st field and the above-mentioned external lead portion serve as a flat continuous field. A level difference is prepared in the 2nd field of the above-mentioned lead, and the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. It is [0012] by which the 2nd field of the above and an outer edge surface expose the above-mentioned external lead portion from the resin-seal section, the above-mentioned internal lead portion is connected with a semiconductor chip through a bump in respect of the 1st, and the resin seal of the 2nd field is carried out to the above-mentioned resin-seal circles.
[Function] Since the component-side product which the external lead was settled in the area which the closure resin section of a semiconductor device occupies, and was needed with projection of the conventional external lead is

reducible according to the means mentioned above, it becomes possible to raise the mounting efficiency in substrate mounting of a semiconductor device.
[0013] Hereafter, the composition of this invention is explained with an example.
[0014] In addition, in the complete diagram for explaining an example, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0015]
[Example] Drawing 1 is for explaining the structure of the semiconductor device which is one example of this invention.
[0016] The semiconductor device of this example shown in drawing 1 is a rectangle type, and shows the side elevation seen from the rectangular shorter side side to drawing 2 , the side elevation seen from the long side side to drawing 3 , and the plan seen from the base to drawing 4 , respectively.
[0017] In drawing 1 - drawing 4 , in a bump and 3, a chip and 4 show the resin-seal section and 5 shows [1 / an internal lead portion and 2] an external lead portion, respectively.
[0018] As the semiconductor device of this example is shown in drawing 1 , the level difference is prepared in the lead and in case a lead is mounted in the internal lead portion 1, a substrate, etc. which make connection with a semiconductor chip 3, it consists of an external lead portion 5 which functions as an end-connection child of a semiconductor device. In addition, in this application, the thin portion of the method of the inside of a lead is used as the internal lead portion 1 in drawing 1 , the thick portion of the method of the outside of a lead is used as the external lead portion 5, and the external lead portion 5 is partially exposed from the resin-seal section 4. [0019] The level difference of this lead is obtained by carrying out half dirty [of the internal lead portion 1 of a lead], or sticking two leads and cutting them in a completely different class.
[0020] The bump 2 who consists of solder is formed on the internal lead portion 1 in the resin-seal section 4, and it connects with the semiconductor chip 3 electrically through the bump 2. In addition, you may be the bump who prepared in the semiconductor chip 3 side beforehand as a means to connect electrically the internal lead portion 1 and semiconductor chip 3 at this time.
[0021] And field attachment mounting of the external lead portion 5 which projects from the resin-seal section 4 shown in drawing 2 - drawing 4 is carried out at a substrate etc.
[0022] Thereby, it becomes possible conventionally only for the part of the external lead projected from the lateral portion of the resin-seal section 4 to reduce a mounting space, or to assign mounting of other parts etc.
[0023] Next, the leadframe of the semiconductor device of this example is explained using drawing 5 .
[0024] In drawing 5 , the bump who joins a semiconductor chip with larger 3A, a semiconductor chip with smaller 3B, a semiconductor chip with larger 2A, and an internal lead portion, and the bump who joins a semiconductor chip and an internal lead portion with larger 2B are shown, respectively.
[0025] In [an internal lead emanating], as shown in drawing 5 , the configuration of the leadframe of the semiconductor device of this example has spread from near the center of a frame.
[0026] When this carries larger semiconductor chip 3A which is the semiconductor chip of different size shown with the dashed line, or when it carries smaller semiconductor chip 3B, the pad position of each semiconductor chips 3A and 3B is changed into the connectable position on the internal lead 1, and semiconductor chips 3A and 3B and the internal lead portion 1 can be connected by preparing bump 2A and 2B in the position. The electric connection with the interna lead and semiconductor chip by this bump application is a useful means which is not acquired in wire connection.
[0027] that is, even the leadframe of this example comes out and various semiconductor chips can be applied
[0028] Next, other examples of this invention are shown in drawing 6 and drawing 7 .
[0029] The example of the semiconductor device shown in drawing 6 loses the level difference of the internal lead portion 1 of a semiconductor device, and an external lead portion shown in above-mentioned drawing 1 , and has established the lead which common-use-ized the internal lead and the external lead. namely, -- according to this example -- about [of the board thickness of a lead] -- two thirds embeds by resin -- having -- the lead 1 embedded principal plane (upper surface) -- the electrical installation section with a semiconductor chip -- nothing -- on the other hand -- about [of the board thickness of a lead] -- one third -- the exposure from resin -- the -- it exposed and also a principal plane serves as an end-connection child to a mounting substrate, and a jamming external lead
[0030] Thereby, a thin shape-ized package is obtained while the substrate and the area of the contact portion of an external lead at the time of mounting are securable. It becomes unnecessary to attach a level difference to a leadframe.
[0031] The example of the semiconductor device shown in drawing 7 forms the fin 6 for heat dissipation on the semiconductor chip 3 of the semiconductor device shown in above-mentioned drawing 1 , and misses the heat emitted from a semiconductor chip.

[0032] In addition, although the rectangle type semiconductor device was taken, respectively and this example mentioned it, it is the same also about a square type semiconductor device.
[0033] Moreover, although the semiconductor device of the COL (CHIP ON LEAD) structure of this example took an gave the example which made the base shell external lead project, it makes an upper surface shell external lead project in semiconductor devices, such as LOC (LEAD ONCHIP) structure.
[0034]
[0035] As mentioned above, although invention made by this invention person was concretely explained based on the aforementioned example, this invention of the ability to change variously in the range which is not limited to the aforementioned example and does not deviate from the summary is natural.
[0036]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0037] A lead has a semiconductor chip, the 1st field which counters, and the 2nd field used as the rear face of this 1st field. The internal lead portion of the 1st field and the above-mentioned external lead portion serve as a flat continuous field. A level difference is prepared in the 2nd field of the above-mentioned lead, and the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. The 2nd field of the above and an outer edge surface expose the above-mentioned external lead portion from the resin-seal section. the above-mentioned internal lead portion By composition it connects with a semiconductor chip through a bump in respect of the 1st, and the resin seal of the 2nd field is carried out [composition] to the above-mentioned resin-seal circles An external lead is settled in the area which the closure resin section of a semiconductor device occupies, and since the component-side product which was needed with projection of the conventional external lead is reducible, it becomes possible to raise the mounting efficiency in substrate mounting of a semiconductor device.

[Translation done.]

* NOTICES *

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CLAIMS

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(57) [Claim(s)]

[Claim 1] The semiconductor chip by which a resin seal is carried out. Two or more leads with which the external lead portion and the internal lead portion were united, and the resin-seal section. The 1st field where it is the semiconductor device equipped with the above, and the above-mentioned lead counters with a semiconductor chip, Have the 2nd field used as the rear face of this 1st field, and the internal lead portion of the 1st field and the above-mentioned external lea portion serve as a flat continuous field. A level difference is prepared in the 2nd field of the above-mentioned lead, anc the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. It is characterized by for the 2nd field of the above and an outer edge surface exposing the above-mentioned external lead portion from the resin-seal section, connecting the above-mentioned internal lead portion with a semiconductor chip in respect of th 1st, and carrying out the resin seal of the 2nd field to the above-mentioned resin-seal circles.

[Claim 2] The semiconductor chip by which a resin seal is carried out. Two or more leads with which the external lead portion and the internal lead portion were united, and the resin-seal section. The 1st field where it is the semiconductor device equipped with the above, and the above-mentioned lead counters with a semiconductor chip, Have the 2nd field used as the rear face of this 1st field, and the internal lead portion of the 1st field and the above-mentioned external lea portion serve as a flat continuous field. A level difference is prepared in the 2nd field of the above-mentioned lead, anc the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. It is characterized by for the 2nd field of the above and an outer edge surface exposing the above-mentioned external lead portion from the resin-seal section, connecting the above-mentioned internal lead portion with a semiconductor chip through a bump in respect of the 1st, and carrying out the resin seal of the 2nd field to the above-mentioned resin-seal circles.

[Claim 3] The semiconductor chip by which a resin seal is carried out. Two or more leads with which the external lead portion and the internal lead portion were united, and the resin-seal section. The 1st field where it is the semiconductor device equipped with the above, and the above-mentioned lead counters with a semiconductor chip, Have the 2nd field used as the rear face of this 1st field, and the internal lead portion of the 1st field and the above-mentioned external lea portion serve as a flat continuous field. By carrying out half dirty to the 2nd field of the above-mentioned lead, a level difference is prepared and the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. It is characterized by for the 2nd field of the above and an outer edge surface exposing the above-mentioned external lead portion from the resin-seal section, connecting the above-mentioned internal lead portion with a semiconductor chip in respect of the 1st, and carrying out the resin seal of the 2nd field to the above-mentioned resin-seal circles.

[Claim 4] The semiconductor device according to claim 3 characterized by connecting electrically through a bump in case the above-mentioned semiconductor chip and an internal lead portion are connected electrically.

[Claim 5] The semiconductor chip by which a resin seal is carried out. Two or more leads with which the external lead portion and the internal lead portion were united, and the resin-seal section. The 1st field where it is the semiconductor device equipped with the above, and the above-mentioned lead counters with a semiconductor chip, Have the 2nd field used as the rear face of this 1st field, and the internal lead portion of the 1st field and the above-mentioned external lea portion serve as a flat continuous field. A level difference is prepared in the 2nd field of the above-mentioned lead, anc the above-mentioned internal lead portion is thinner than the above-mentioned external lead portion. The 2nd field of the above and an outer edge surface expose the above-mentioned external lead portion from the resin-seal section. the above-mentioned internal lead portion It has spread in the radial focusing on the above-mentioned semiconductor chip, connects with a semiconductor chip electrically through a bump in the proper position of the 1st field corresponding to the pad of a semiconductor chip, and is characterized by carrying out the resin seal of the 2nd field to the above-mentioned resin-seal circles.

[Translation done.]

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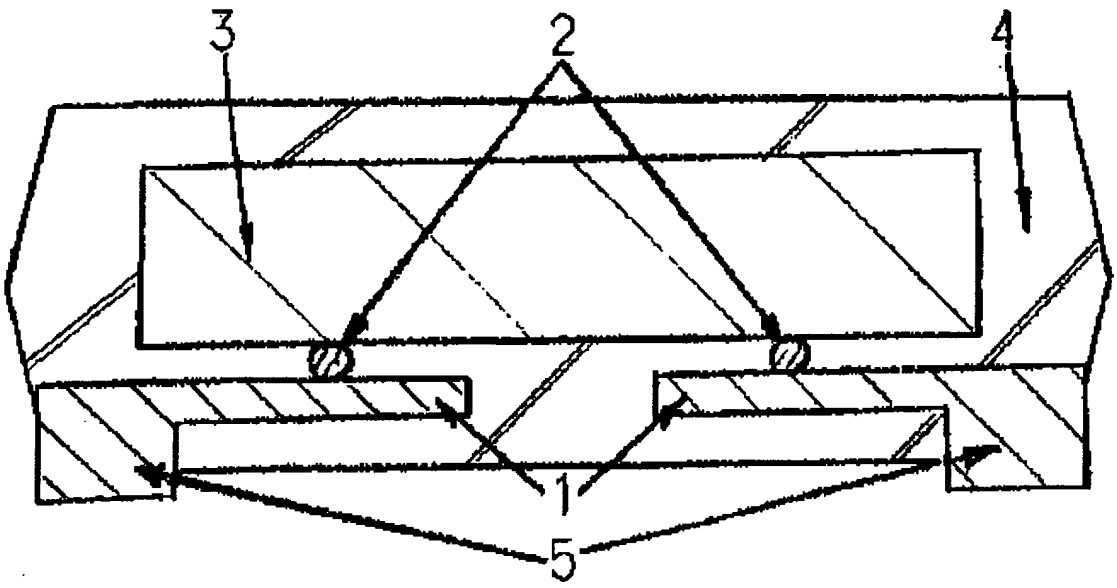
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing for explaining the structure of the semiconductor device which is one example of this invention.
[Drawing 2] It is the side elevation of the semiconductor device of this example.
[Drawing 3] It is the side elevation of the semiconductor device of this example.
[Drawing 4] It is the plan seen from the base of the semiconductor device of this example.
[Drawing 5] It is drawing for explaining the structure of the leadframe in the semiconductor device of this example.
[Drawing 6] It is drawing for explaining the structure of the semiconductor device which are other examples of this invention.
[Drawing 7] It is drawing for explaining the structure of the semiconductor device which are other examples of this invention.
[Description of Notations]
1 [-- A chip, 4 / -- The resin-seal section, 5 / -- An external lead portion, 6 / -- Fin for thermolysis.] -- An internal lead portion, 2 -- A bump, 3

[Translation done.]

図 1



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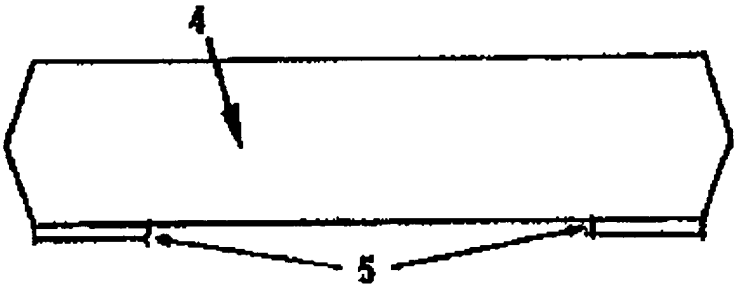

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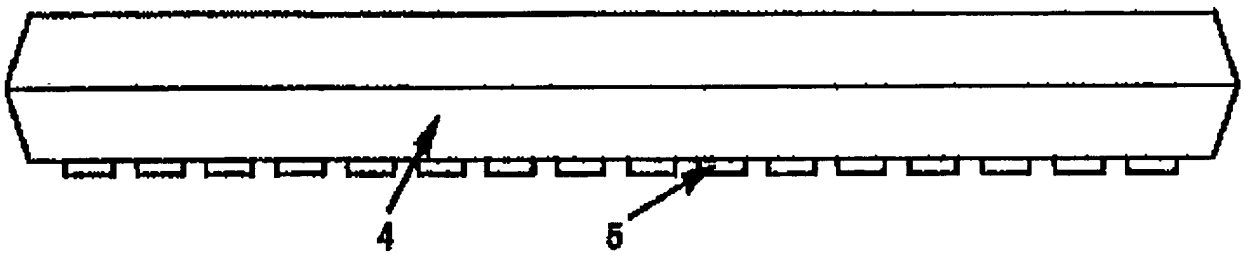

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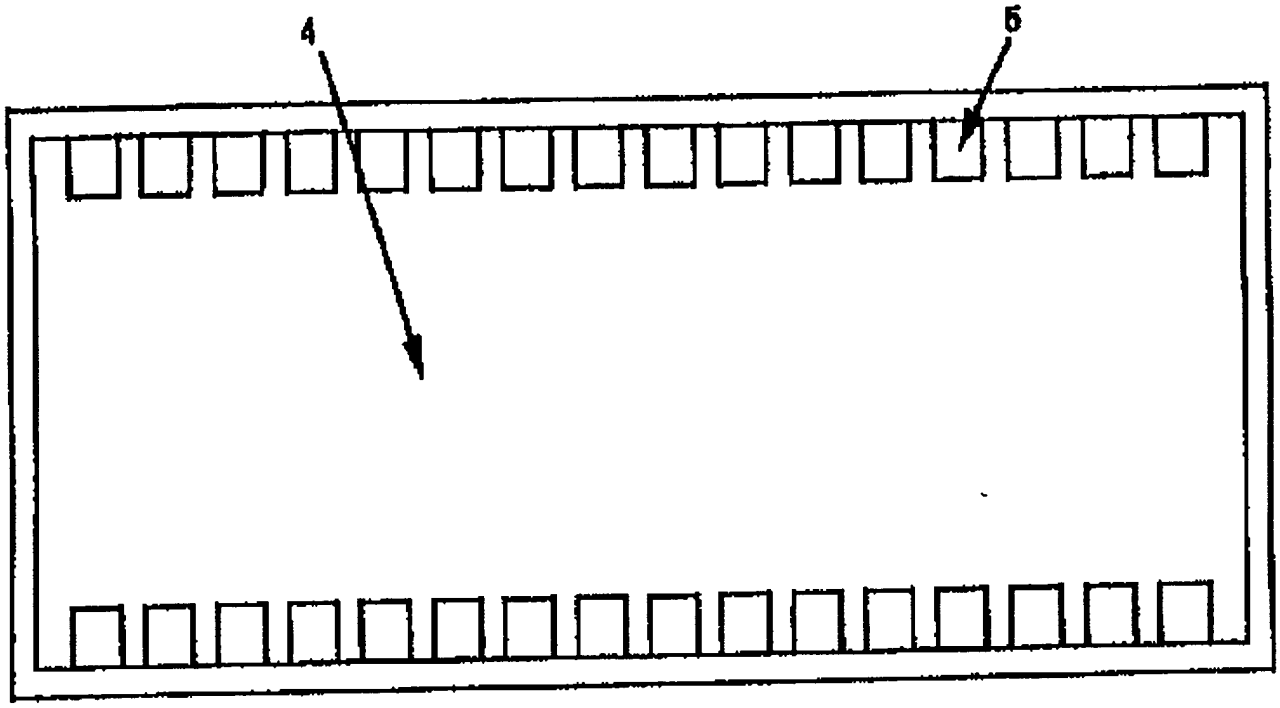

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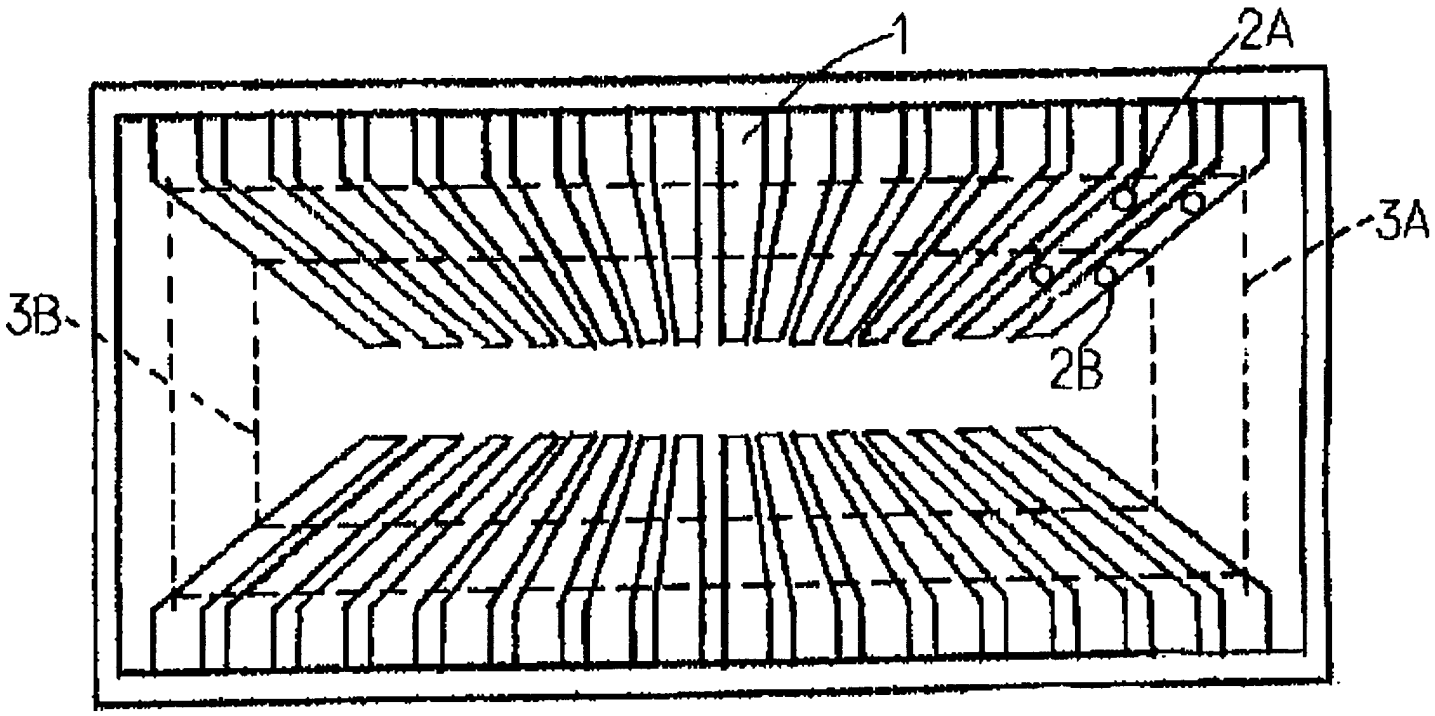

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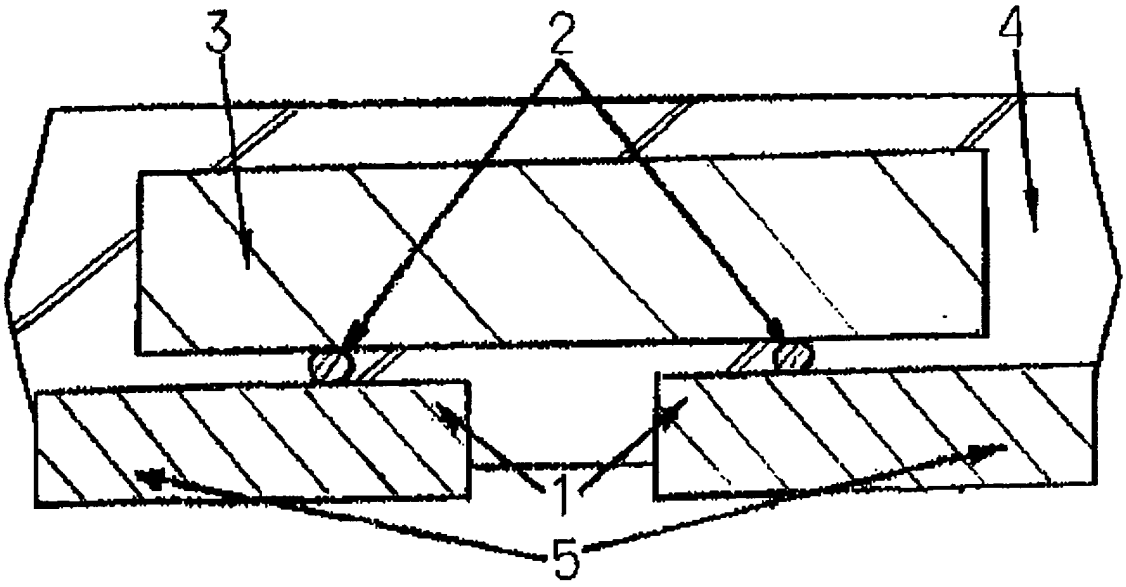

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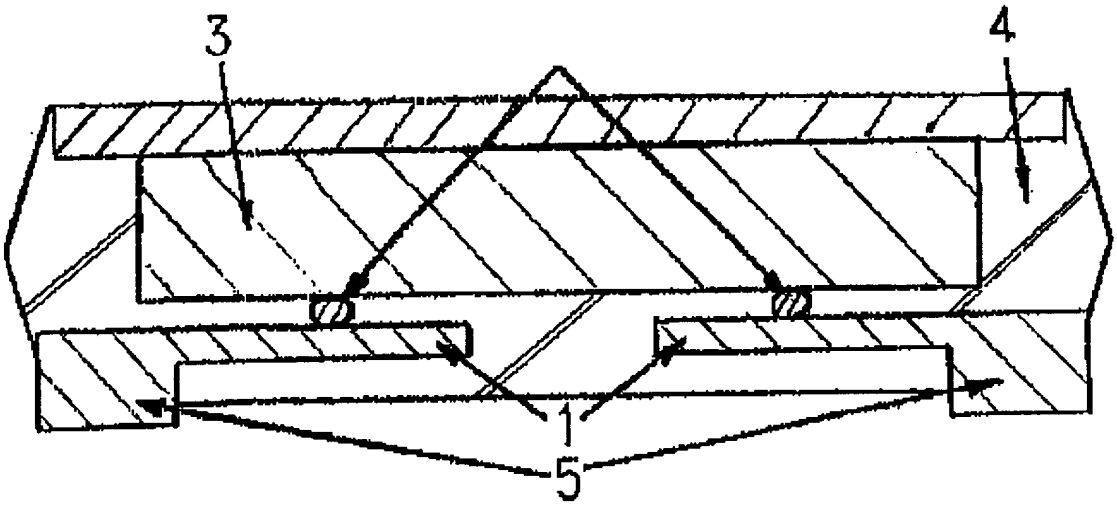

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/13364

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/495 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 794 572 A (MATSUSHITA ELECTRONICS CORP) 10 September 1997 (1997-09-10) the whole document ---	1-36
X	US 5 521 429 A (AONO TSUTOMU ET AL) 28 May 1996 (1996-05-28) abstract ---	1-36
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 358 (M-1633), 6 July 1994 (1994-07-06) & JP 06 092076 A (OKI ELECTRIC IND CO LTD), 5 April 1994 (1994-04-05) abstract ---	1-36
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[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
6 October 1999	15/10/1999

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/13364

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 087 (E-393), 5 April 1986 (1986-04-05) & JP 60 231349 A (TOSHIBA KK), 16 November 1985 (1985-11-16) abstract	1-36
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2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/13364

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